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ANALYSIS OF ADIABATIC CIRCUIT APPROACH FOR ENERGY RECOVERY LOGICS

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ABSTRACT

Adiabatic logic, which works on the principle of Energy Recovery, is proving to be an emerging low power approach in low power design. A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Just losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

KEYWORDS: Adiabatic, ECRL, PFAL, Secure logic.

INTRODUCTION

The demand for portable electronic gadgets which are small reliable and with a long battery life has led to rampant scaling which has led to the reduction in feature size of the device and the ill effect of this process has led to an increase in leakage power dissipation even when the device is non operational.

Various techniques have been evolved over the years to counter the increase in leakage power. Each technique has its own advantage and disadvantage for its application.In adiabatic circuits, energy dissipation can he separated two parts. One is an adiabatic loss**;** the other is a non- adiabatic loss.When a current flow through the transistor, an adiabatic loss is generated by switching resistance of transistor. That is related with the operating frequency. In adiabatic charging, the increase of a transition time will result in decrease of energy loss. But we can't avoid an adiabatic loss**.** This loss is not related with operating frequency but to the voltage drop, the node capacitance and the cascading time. We can reduce the non-adiabatic loss by several techniques like logic families, the Efficient Charge Recovery Logic (ECRL), the Positive Feedback Adiabatic Logic(PFAL) and the 2N-2N2P are studied with respect to energy saving

EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

In order to recover and to reuse the supplied energy, an ac power supply is used for ECRL gate.

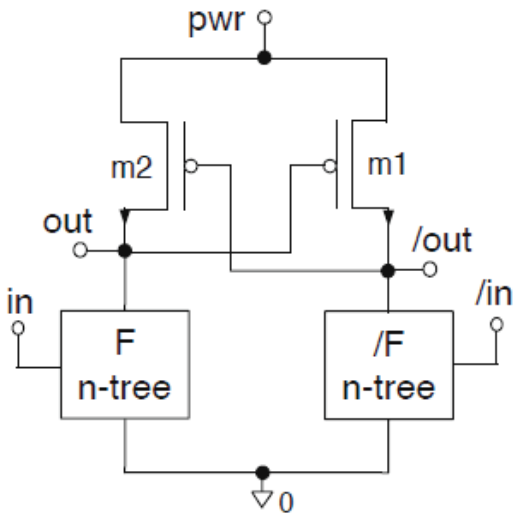


Figure1 Basic ECRL Structure

ECRL structure uses a pair of pull down NMOS transistors to evaluate functions and a pair of cross coupled PMOS device to hold the charges. If the circuit operates correctly, energy has an oscillatory behavior, because a large part of the energy supplied to the circuit is given back to the power supply, as shown in figure 1.

As usual for adiabatic logic the energy behavior follows the supply voltage. In the same figure we may observe that, due to a coupling effect, the low level output goes to a negative voltage value during the recovery phase(that is, when the supply voltage ramps down). We define “Dissipated Energy" as the difference between the energy that the circuit needs to load the output capacitance, and the energy that the circuit gives back to the power supply during the recovery phase.

The dissipated energy value depends on the input sequence and on the switching activity factors; therefore the dissipated energy per cycle can be obtained from the mean value of the whole sequence. It can also be seen that a larger energy is dissipated if the input state changes and therefore the output capacitances have to switch[1].

POSITIVE FEEDBACK ADIABATIC LOGIC (PAFL)

Two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission pMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in Figure2. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied
energy decreases[2].

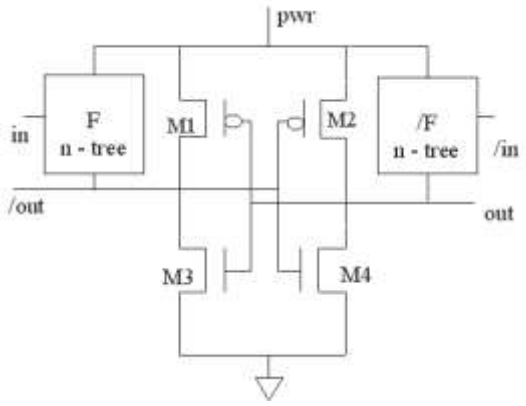


Figure 2 Basic PAFL structure

N-2N2P

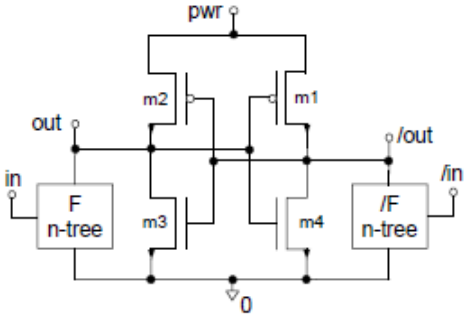
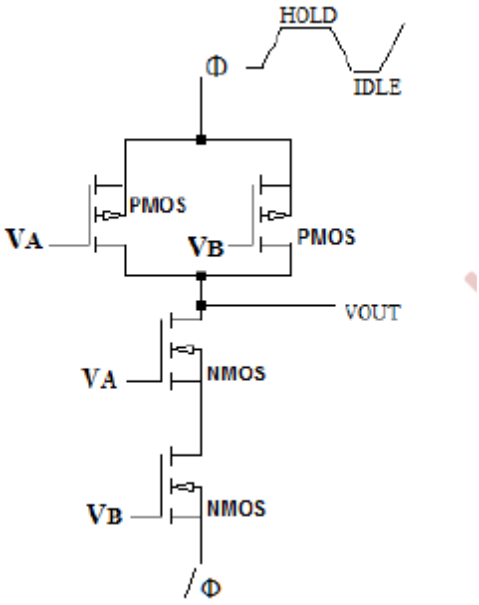


Figure 3 Basic structure of 2n-2n2p

This adiabatic logic family was derived from ECRL in order to reduce the coupling effect. Figure 3 shows the general schematic. The primary advantage of 2N-2N2P over ECRL is that the cross-couple NMOS switches result in non-floating outputs for large part of the recovery phase. The new NMOSs also have the advantage of eliminating floating nodes in the system, which prevents charge leakage. However, the added transistors prevent it from achieving significant energy savings at speeds above 100 MHz[2].

SPLIT LEVEL CHARGE RECOVERY LOGIC



The inverter is driven by two complementary power clocks Φ and / Φ rather than Vdd and ground terminals. Fig 4.clearly explains that the power clock input Φ varies between Vdd and Vdd/2 whereas /Φ varies between Vdd/2 and 0. Initially all the nodes (Φ and / Φ) are at Vdd/2, at that time the transmission gate is turned OFF by the clocks P and /P and the output is also at Vdd/2. After a valid input is applied the transmission gate at the output is gradually turned ON by swinging P and /P to Vdd and ground respectively. Then clock Φ and / Φ swing to Vdd to ground respectively. If the input to the gate is Vdd then the node marked x and the output will follow / Φ and ground and if the input was at ground the node x and output follow Φ and Vdd [5]**.**

TWO PHASE ADIABATIC STATIC CLOCKED LOGIC

The Two Phase Adiabatic Static Clocked Logic (2PASCL) uses two phase clocking split level sinusoidal power supply's which has symmetrical and asymmetrical power clocks where one clock is in phase while the other is out of

phase.The circuit has two diodes in its construction where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. The circuit operation is divided into two phases "hold phase" and "evaluation phase". During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down [6].

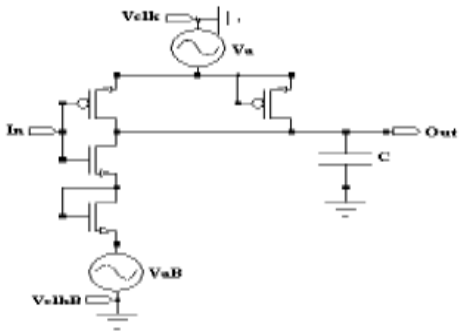


Figure 5 Structure of two phased clock adiabatic logic

SECURE ADIABATIC LOGIC

The basic structure of an SAL gate is shown in Fig. 6(a). It consists of three main parts:
i) Two function blocks which construct the outputs. These functions are implemented by NMOS transistors.
ii) A latch which is made by two cross-coupled PMOS transistors, i.e., MP1 and
MP2. Also, two cross-coupled NMOS transistors, i.e., MN1 and MN2, are inserted to cause that the outputs not to be float. This latch saves the value of out signals when the inputs fall down. Falling the inputs down before the outputs is unavoidable in all adiabatic logic styles.
iii) Extra pass transistors, i.e., MN3 to MN8, that are responsible to discharge
internal capacitances of the function blocks adiabatically. In fact, this part is added to recover the energies locked up in internal capacitances. Therefore, it leads to reduce the data-dependent dynamic power consumption.[3]

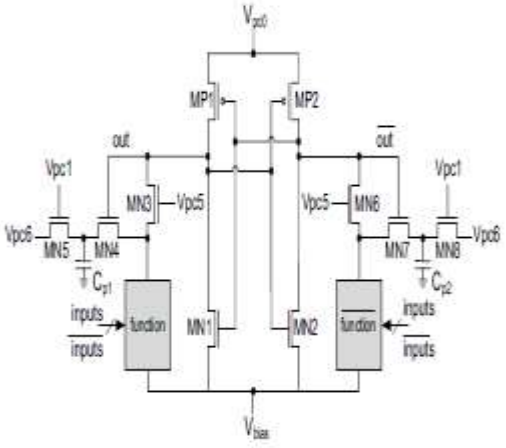


Figure 6(a) Basic structure of secure adiabatic logic

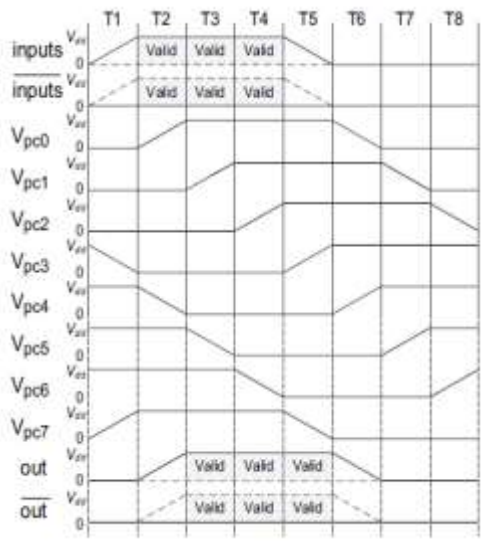


Figure 6(b) Timing diagram of secure adiabatic logic
According to Fig. 6(b) each SAL gate operates in eight phases:

T1- In this phase, input signals can change and will be valid at the end of the phase. Thus, one of the function blocks turns on according to the input values. Also, in this phase Vpc5 is HI and Vpc1 is LO. So MN3 and MN6 are on; MN5 and MN8 are off. Thus, the output of function blocks are connected to out signals.

T2- During this phase Vpc0 goes HI steadily, and out signals are evaluated. Other signals remain unchanged within this phase. At the end of this phase out signals take their valid values and remain valid for next three phases because cross-coupled PMOS transistors keep them while Vpc0 is HI.

T3- Simultaneously Vpc1 and Vpc5 go steadily HI and LO respectively. Thus, MN5 and MN8 will be on. Also, MN3 and MN6 will be off, and it will be possible to recover the energy stored in the internal capacitances of function blocks without affecting the output validity.

T4- In this phase the energy stored in the internal capacitances of a function block is recovered. Vpc6 goes LO steadily, and the stored energy is recovered via two transistors: “MN4 and MN5” or “MN7 and MN8”. At the end of this phase, the capacitance of all nodes except one of out signals is discharged.

T5- During this phase, all of HI input signals go LO and turn function blocks off. All other signals remain unchanged during this phase.

T6- Vpc0 goes LO, and the energy stored in one of load capacitances is recovered
through a PMOS transistor, i.e., MP1 or MP2. As mentioned previously, the charge recovery process continues till Vtp.

T7- Vpc1 and Vpc5 go steadily LO and HI respectively. Thus, output of the function blocks are disconnected from Vpc6, and each one is connected to the corresponding out signal.

T8- Vpc6 goes HI, and at the end of this phase all parts of the circuit will be as same as the start of the first phase.

i) The function blocks and the two cross-coupled NMOS transistors are connected to a DC bias voltage equal to Vtp instead of GND. Note that the bulk of NMOS transistors are already connected to GND. It avoids the non-adiabatic energy dissipation due to incomplete discharge of Cload.

ii) A mechanism was employed to recover the energies stored in the internal parasitic capacitances of the function blocks. It was achieved by adding some extra pass transistors, i.e., MN3 to MN8, and applying some modifications

on the timing of the circuit in comparison with other charge recovery logic styles.This mechanism aim at avoiding the data-dependent dissipation[3].

CONCLUSION

The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

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